STANSON

STP4441

P Channel Enhancement Mode MOSFET

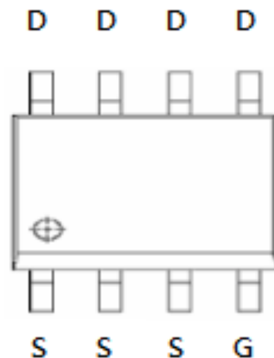
-10.0A

DESCRIPTION

STP4441 is the P-Channel logic enhancement mode power field effect transistor which is produced using high cell density, DMOS trench technology. The STP4441 has been designed specially to improve the overall efficiency of DC/DC converters using either synchronous or conventional switching PWM controllers. It has been optimized for low gate charge, low $R_{DS(ON)}$ and fast switching speed.

PIN CONFIGURATION

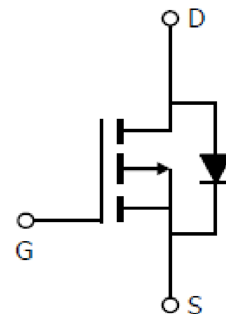
SOP-8



FEATURE

- -60V/-10.0A, $R_{DS(ON)}$ = 55mΩ（Typ.） @V_{GS} = -10V
- -60V/-5.0A, $R_{DS(ON)}$ = 73mΩ（Typ.） @V_{GS} = -4.5V
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability
- SOP-8 package design

PART MARKING



Y：Year Code
A：Date Code
B：Process Code
C：Wafer Code

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www.stansontech.com

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ABSOULTE MAXIMUM RATINGS (Ta = 25℃ Unless otherwise noted)

Parameter		Symbol	Typical	Unit
Drain-Source Voltage		VDSS	-60	V
Gate-Source Voltage		VGSS	±20	V
Continuous Drain Current (TJ=150℃)	TA=25℃ TA=100℃	ID	-10.0 -4.0	A
Pulsed Drain Current		IDM	-40	A
Continuous Source Current (Diode Conduction)		IS	-3	A
Power Dissipation	TA=25℃ TA=70℃	PD	2.3 1.3	W
Operation Junction Temperature		TJ	-55/150	℃
Storgae Temperature Range		TSTG	-55/150	℃
Thermal Resistance-Junction to Ambient		RθJA	70	℃/W

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ELECTRICAL CHARACTERISTICS (Ta = 25℃ Unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS}=0V,ID=-250uA	-60			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS},ID=-250uA	-1.0		-2.5	V
Gate Leakage Current	I_{GSS}	V_{DS}=0V,V_{GS}=±20V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=-48V,V_{GS}=0V			-1	uA
		V_{DS}=-48V,V_{GS}=0V T_J=85℃			-10	uA
On-State Drain Current	$I_{D(on)}$	V_{DS}≧-10V,V_{DS}=-5V	-10			A
Drain-source On-Resistance	$R_{DS(on)}$	V_{GS}=-10V,I_D=-10A V_{GS}=-4.5V,I_D=-5A		53 71	60 81	mΩ
Forward Transconductance	gfs	V_{DS}=-5V,I_D=-10A		18		S
Diode Forward Voltage	V_{SD}	I_S=-2.3A,V_{GS}=0V		-0.7	-1.0	V
Dynamic						
Total Gate Charge	Q_g	V_{DS}=-30V,V_{GS}=-10V I_D=-5A		47	55	nC
Gate-Source Charge	Q_{gs}			5.8		nC
Gate-Drain Charge	Q_{gd}			9.3		nC
Input Capacitance	C_{iss}	V_{DS} =-30V,V_{GS}=0V F=1MHz		2410		pF
Output Capacitance	C_{oss}			197		pF
Reverse TransferCapacitance	C_{rss}			125		pF
Turn-On Time	$t_{d(on)}$	V_{GS}=-10V,V_{DS}=-30V R_{EGN}=3Ω,R_L=4.7Ω		9		nS
	tr			6.2		nS
Turn-Off Time	$t_{d(off)}$			25		nS
	tf			11		nS

TYPICAL CHARACTERICTICS

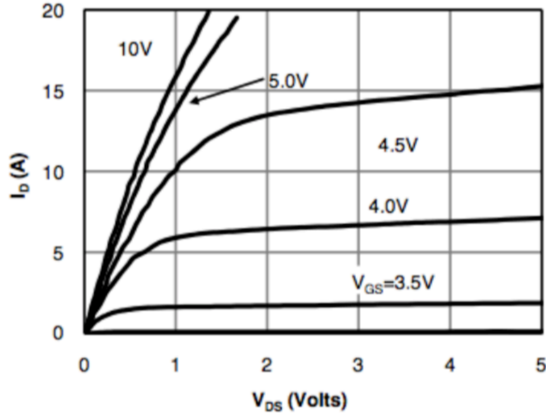

Fig 1: On-Region Characteristics

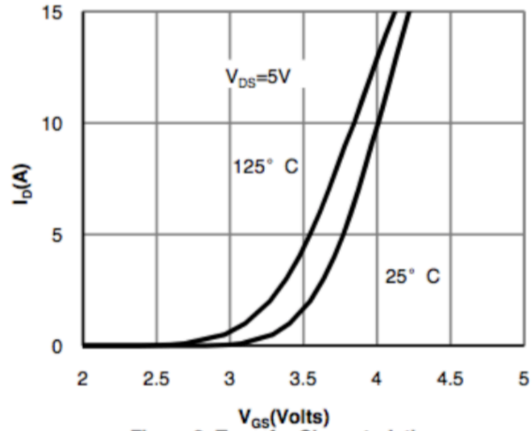

Figure 2: Transfer Characteristics

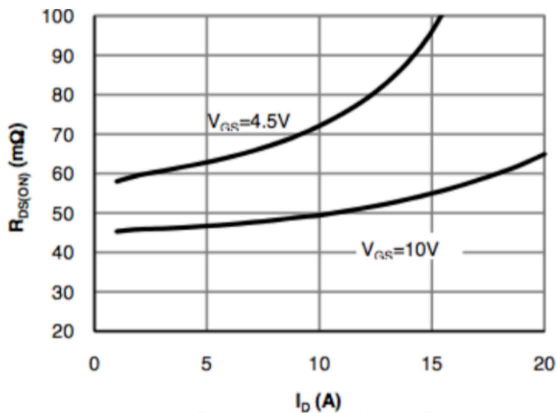

Figure 3: On-Resistance vs. Drain Current and Gate Voltage

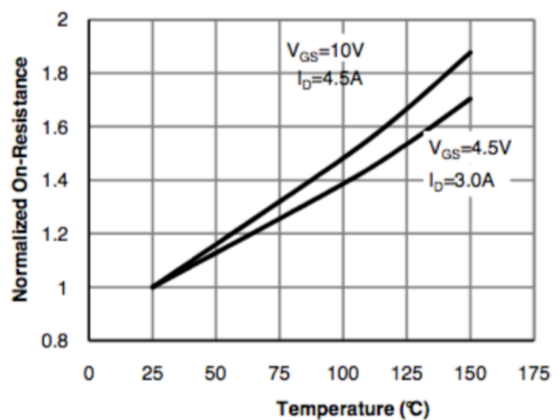

Figure 4: On-Resistance vs. Junction Temperatu

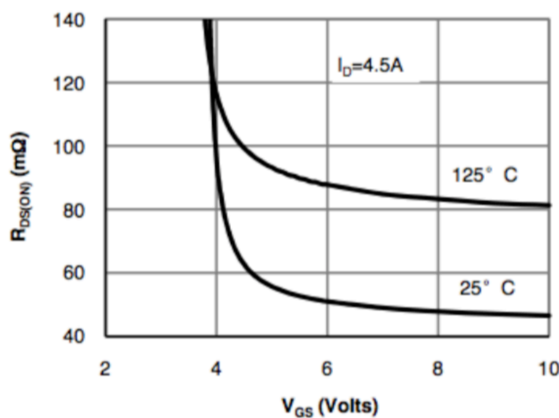

Figure 5: On-Resistance vs. Gate-Source Voltage

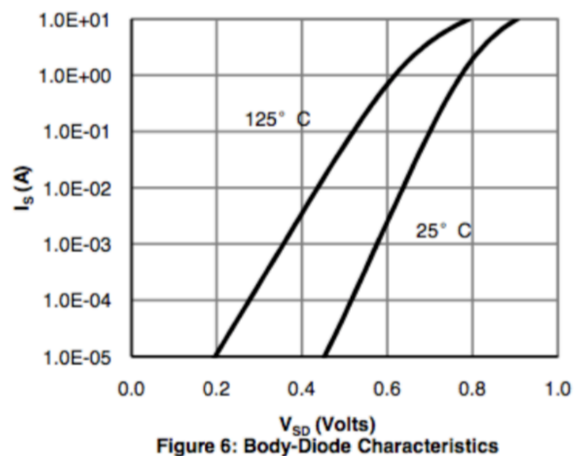

Figure 6: Body-Diode Characteristics

TYPICAL CHARACTERICTICS

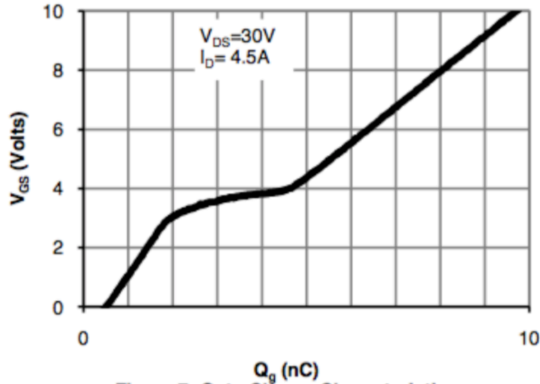

Figure 7: Gate-Charge Characteristics

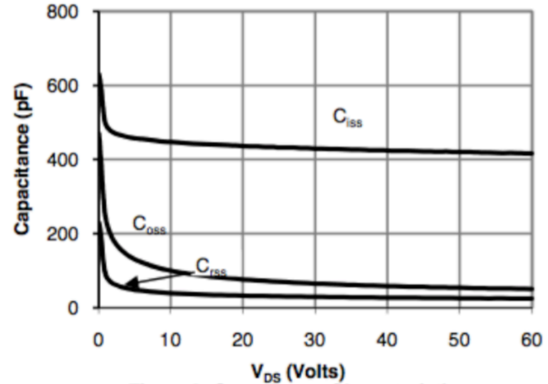

Figure 8: Capacitance Characteristics

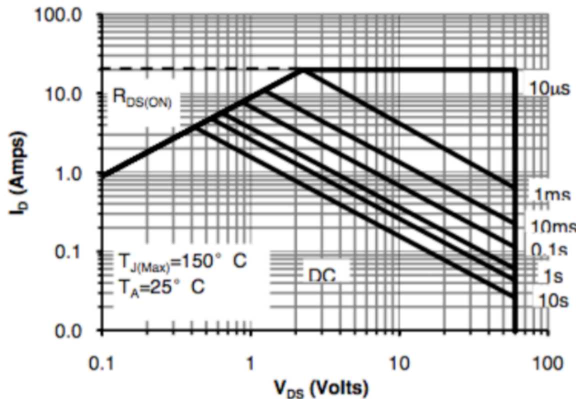

Figure 9: Maximum Forward Biased Safe Operating Area (Note E)

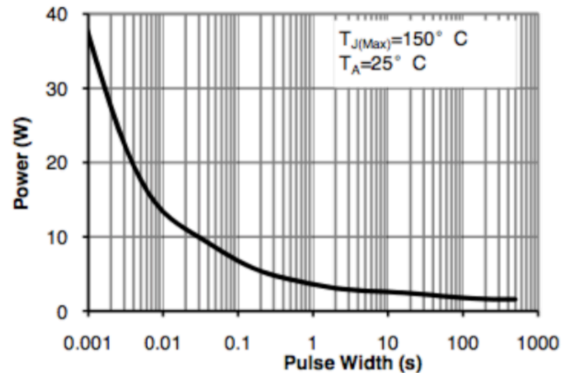

Figure 10: Single Pulse Power Rating Junction-Ambient (Note E)

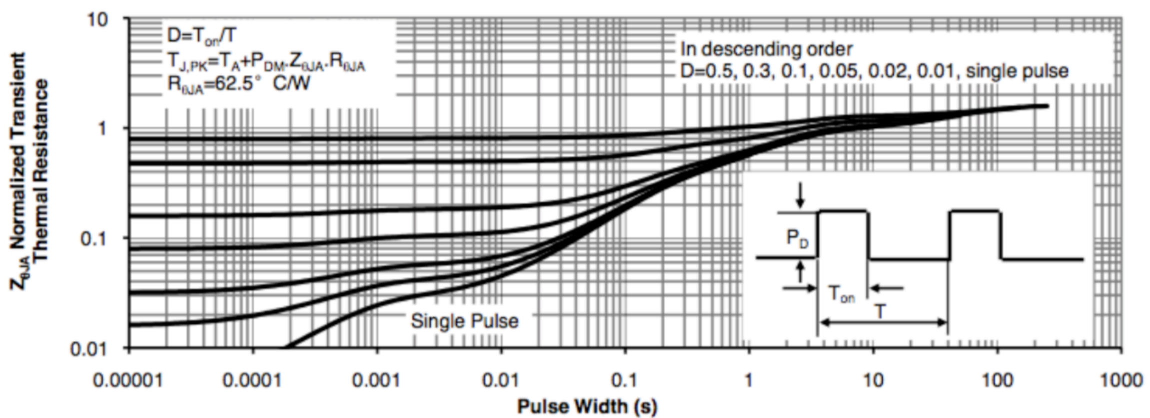

Figure 11: Normalized Maximum Transient Thermal Impedance

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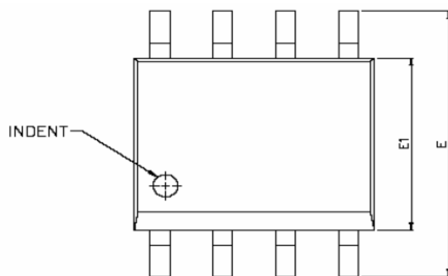
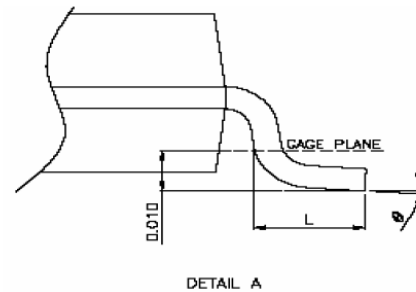
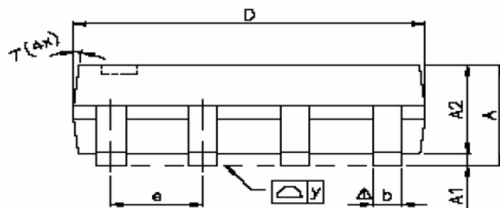
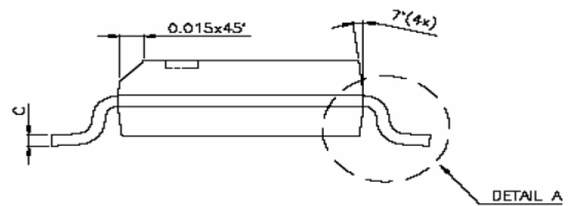
SOP-8 PACKAGE OUTLINE









SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.47	1.60	1.73	0.058	0.063	0.068
A1	0.10	——	0.25	0.004	——	0.010
A2	——	1.45	——	——	0.057	——
b	0.33	0.41	0.51	0.013	0.016	0.020
C	0.19	0.20	0.25	0.0075	0.008	0.0098
D	4.80	4.85	4.95	0.189	0.191	0.195
E	5.80	6.00	6.20	0.228	0.236	0.244
E1	3.80	3.90	4.00	0.150	0.154	0.157
e	——	1.27	——	——	0.050	——
L	0.38	0.71	1.27	0.015	0.028	0.050
⚠2 y	——	——	0.076	——	——	0.003
θ	0°	——	8°	0°	——	8°